AGILE CONDOR® HIGH-PERFORMANCE EMBEDDED COMPUTING

The *Agile Condor* system brings **supercomputing to the edge**, analyzing vast quantities of data to reveal real-time actionable intel

SRC is bringing big data analysis closer to the sensor. Intelligence, surveillance and reconnaissance (ISR) systems are now able to collect vast quantities of data that must be analyzed to provide mission critical intel. Currently, data is either stored and downloaded for review at the end of the mission, or downloaded in-mission through a data link, creating unacceptable latency between data collection and analysis.

SRC's *Agile Condor*® high-performance embedded computing (HPEC) architecture reduces this timeline by enabling processing, exploitation and dissemination (PED) directly at the sensor in extremely size, weight and power (SWaP) constrained environments.

TERAFLOPS OF PROCESSING POWER AT THE EDGE

The *Agile Condor* system was developed by SRC for the Air Force Research Lab (AFRL) in Rome, NY. The system is a scalable, low cost, size, weight and power (low-CSWaP) computing architecture that supports the use of commercial off-the-shelf (COTS) single-board computers (SBCs), graphics processing units (GPUs), Field-Programmable Gate Arrays (FPGAs), and solid-state storage devices (SSDs).

The system leverages a modular, distributed network of processors and co-processors based on open industry standards to deliver teraflops of computational power at gigaflops per watt.

Upgradability and reliability
The COTS upgradeable architecture of the *Agile Condor* system enables extremely fast technology refresh, simultaneously decreasing life cycle costs, reducing system downtime, and assuring continued effectiveness/ operability of the system.

LOW-SWAP DESIGN

The low-SWaP hardware can be mounted in a variety of configurations to meet the needs of any mission. Initially developed for use in an airborne pod, the system excels at bringing supercomputer levels of processing power to confined spaces with minimal power. Its low-SWAP design allows the *Agile Condor* system to operate in a variety of environments – in the air on remotely piloted aircraft (RPA), on land vehicles or fixed site locations, at sea, and even in space.

NEUROMORPHIC COMPUTING AND MACHINE LEARNING

The modular design of the *Agile Condor* system's architecture allows for expandable computational power, paving the way for advanced neuromorphic and machine learning computing technology.

THE AGILE CONDOR HPEC ARCHITECTURE PROCESSES TERAFLOPS OF DATA DIRECTLY AT THE SENSOR, GIVING WARFIGHTERS THE COMPETITIVE EDGE IN INTELLIGENCE ANALYSIS

Neuromorphic Computing
Bio-inspired technology like neuromorphic computers function similarly to the human brain - using very little power for certain tasks. Coupled with the *Agile Condor* system, neuromorphic computing would allow RPAs to stay in the air for longer durations – enabling new and more efficient missions.

Top: Actively cooled Agile Condor system
Left: Passively cooled Agile Condor system

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Machine Learning
The *Agile Condor* system leverages machine learning techniques to process data on board, delivering enhanced situational awareness, adaptive decision making, multi-mode, multi-mission, massive analytics and heterogeneous information processing, helping operators to recognize and act on actionable intel in real-time.

Coupled with SRC's optimized, distributed, portable data pipeline software, the *Agile Condor* system can provide assisted autonomy to RPAs. The system also facilitates the processing of data from multiple sensors and utilize machine learning capabilities to selectively cue and dynamically engage sensors for a wide variety of scenarios. This selective "detect, classify and alert" process limits bandwidth, while reducing latency between data collection and data analysis.

Real-time preprocessing of data with the *Agile Condor* system also ensures that all data collected is reviewed quickly, increasing the speed and effectiveness with which operators can make informed decisions based on actionable intel.

BENEFITS

- COTS upgradeable architecture ensures
  - Faster technology refresh
  - Decreased life cycle costs
  - Reduced system downtime
  - Continued effectiveness
- Faster, more accurate data analysis
- Reduces backhaul data bandwidth requirements
- Rapid on board data analysis reduces decision timelines by providing faster access to more actionable intel
- Additional processing at the edge provides options for improved processing, exploitation and dissemination (PED)
- SOSA and OMS aligned, enabling interoperability between systems using open architecture standards

SPECIFICATIONS

- 3U Open VPX design
- Adheres to MIL-STD, IEEE and VITA standards
- 14 slots for compute and storage boards
- Multiple 10GbE I/O connections
- Multiple configurations including airborne pod-based, vehicle mounted and ground-based systems
- Fully ruggedized

FEATURES

- Multi-int processing
- GMTI pattern detection
- FMV object detection and classification
- SAR assisted target detection & classification
- Brings teraflops of processing power to the edge with gigaflops per watt efficiency
- Leverages machine learning and neuromorphic computing techniques
- Modular and scalable design based on open industry standards
- Platform agnostic
- Network centric – able to provide processing power to interconnected distributed systems
- Cascadable to provide increased processing power
- Low power consumption
- Low C-SWaP design

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